REMARKS

Reconsideration of the above-identified application in view of the foregoing amendments and following remarks is respectfully requested.

A. Status of the Claims

Claims 1-3, 5-6 and 9-19 are pending in this application, of which claims 14-19 are withdrawn, i.e., claims 1-3, 5-6 and 9-13 remain under consideration. Claims 1-3, 5-6 and 9-13 stand rejected. By this amendment, claims 1-3, 5-6, 9, 10 and 13 are amended. Support for these claim amendments may be found throughout the application as originally filed including, for example, paragraphs [0058]-[0072] and Figs. 6-7.

No new matter will be introduced into this application by entry of these amendments. Entry is respectfully requested as these amendments place the application in condition for allowance and otherwise reduce matters for appeal.

B. Rejections under 35 U.S.C. § 112

In paragraph two (2) of the Office Action, claims 1-3, 5, 6 and 9-13 have been rejected under 35 U.S.C. § 112, second paragraph, as allegedly being indefinite. The Office Action indicates that several portions of claims 1 and 5 are unclear.

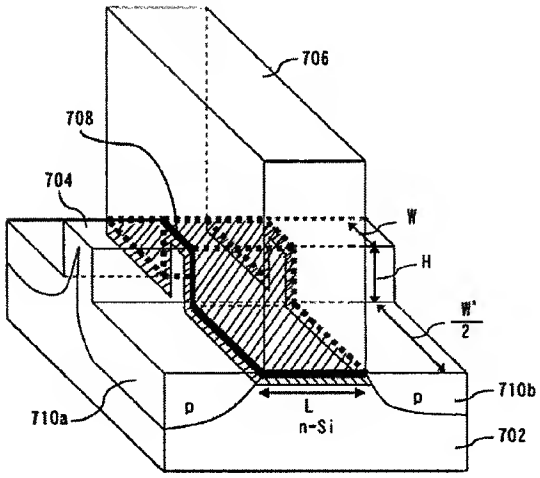
In response, claims 1 and 5 have been amended as shown above addressing the rejections under this category, and Applicants believe that these amendments to claims 1 and 5 overcome the rejections under this category.

Accordingly, reconsideration and withdrawal of the rejections of claims 1-3, 5-6 and 9-13 under 35 U.S.C. § 112, second paragraph, is respectfully requested.

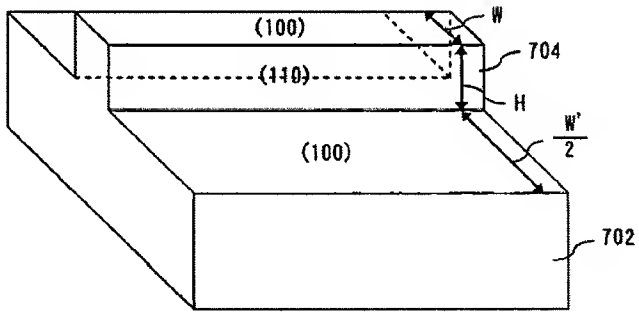
C. Rejections under 35 U.S.C. § 102(b)

In paragraph four (4) of the Office Action, claims 1-3, 5-6 and 9-13 have been rejected under 35 U.S.C. § 102(b) as allegedly being anticipated by U.S. Patent Appl. No. 2003/0102497 to Fried, et al. ("Fried").

Claims 1 and 5 have been amended for further clarification. Amended claim 1 is directed to a MIS transistor comprising a semiconductor substrate having a projecting part, a gate insulator, a gate electrode, and diffusion regions. In particular, the semiconductor substrate of amended claim 1 recites, *inter alia*, "a semiconductor substrate having a surface with a principal crystal plane comprising a projecting part formed directly from the surface of the semiconductor substrate and at least one of a top surface and a side wall of the projecting part has a secondary crystal plane different from the principal crystal plane." Claim 5 has been amended in a similar manner to claim 1 as discussed herein.



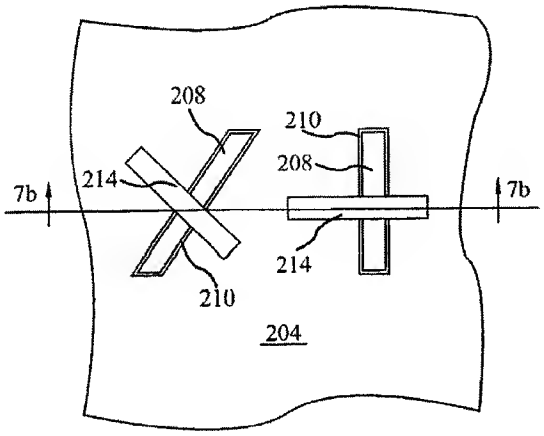
[Applicants, Fig. 6].



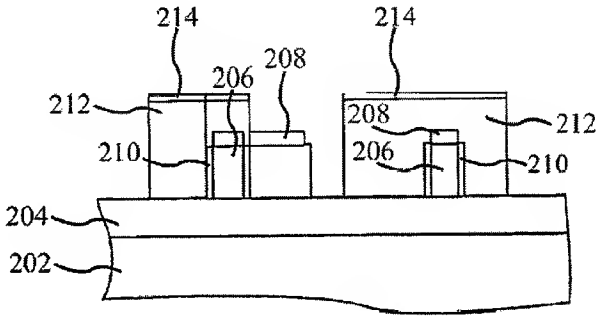
[Applicants, Fig. 7].

Referring to Applicants' Figs. 6 and 7 shown above, the MIS transistor is built on a semiconductor substrate 702 having a projecting part 704 formed directly from the surface of the semiconductor substrate. In particular, the crystal planes of the surface of the semiconductor

substrate, one of the side walls of the projecting part and the top surface of the projecting part in this example is each (100), (110) and (100). In particular, the gate insulator 708 (and the gate electrode 706) of the MIS transistor is formed on the semiconductor substrate in such a way that the gate insulator which defines the channel of the MIS transistor covers a portion of the semiconductor substrate having (100) crystal plane, a portion of the side wall of the projecting part having (110) crystal plane, and a portion of the top surface of the projecting part having (100) crystal plane. In other words, the channel of the MIS transistor is extended by including the side wall of the projecting part having different crystal plane, i.e., the height of the projecting part is included in the width of the channel thereby the driving capacity of the MIS transistor is enhanced. See, e.g., paragraphs [0009] and [0010] of the specification.



[Fried, Fig. 7a].



[Fried, Fig. 7b].

In an effort to optimize the mobility of the electrons in n-channel transistor and the holes in the p-channel transistor which comprise the CMOS FinFET, Fried utilizes different crystal planes for the n-type (NFET) and p-type (PFET) transistors on a common substrate. For example, referring to Figs. 7a and 7b of Fried each illustrate the top and cross-sectional views of the CMOS FinFET as reproduced above, the left-side transistor (e.g., p-channel transistor) may

utilize the (111) crystal plane while the right-side transistor (e.g., n-channel transistor) may utilize the (100) crystal plane. See, e.g., paragraph [0057] of Fried.

In the Response to Arguments section, the Office Action indicates, *inter alia*, that "the elements 208 **& 210** of Fried **are** the gate insulator and the elements cover 'at least a part of **each** of said at least two different crystal planes.'" (emphasis in the original). The same section of the Office Action further indicates that "the element 206 of Fried **are** parts of the SOI substrate, which is comprise of multiple projecting parts (see FIG. 7b)." (emphasis in the original). [7/1/08 Office Action, p. 7]

While Applicants note that element 208 of Fried is not a gate insulator (element 210 is the gate insulator), it appears that the Office Action interprets the utilization of different crystal planes in each of the p-channel and n-channel transistors as 'at least a part of each of said at least two different crystal planes' of claims 1 and 5. However, amended claim 1 recites, *inter alia*, that a gate insulator (i.e., single gate insulator) covers the multiple portions of the same MIS transistor (i.e., semiconductor substrate as well as the top and side wall of the projecting part) having different crystal planes (i.e., principal crystal plane and secondary crystal plane). Additionally, while the projecting part of claims 1 and 5 is formed directly from the surface of the semiconductor substrate (i.e., the projecting part is made of same material as the substrate), the fins 206 of Fried made of silicon are formed on a substrate having different material (i.e., insulator).

Accordingly, each of claims 1 and 5 as amended is believed neither anticipated by nor rendered obvious in view of the cited reference (i.e., Fried) for at least the reasons discussed above.

Reconsideration and withdrawal of the rejections of claims 1 and 5 under 35 U.S.C. § 102(b) is respectfully requested.

Applicants have chosen in the interest of expediting prosecution of this patent application to distinguish the cited documents from the pending claims as set forth above. These statements should not be regarded in any way as admissions that the cited documents are, in fact, prior art. Furthermore, Applicants have not specifically addressed the rejections of the dependent claims. Applicants respectfully submit that the independent claims, from which they depend, are in condition for allowance as set forth above. Accordingly, the dependent claims also are in condition for allowance. Applicants, however, reserve the right to address such rejections of the dependent claims in the future as appropriate.

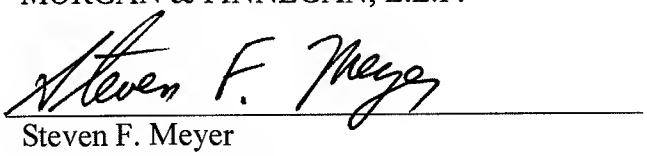
CONCLUSION

For the above-stated reasons, this application is respectfully asserted to be in condition for allowance. An early and favorable examination on the merits is earnestly solicited. In the event that a telephone conference would facilitate the examination of this application in any way, the Examiner is invited to contact the undersigned at the number provided.

THE COMMISSIONER IS HEREBY AUTHORIZED TO CHARGE ANY ADDITIONAL FEES WHICH MAY BE REQUIRED FOR THE TIMELY CONSIDERATION OF THIS AMENDMENT UNDER 37 C.F.R. §§ 1.16 AND 1.17, OR CREDIT ANY OVERPAYMENT TO DEPOSIT ACCOUNT NO. 13-4500, ORDER NO. 5000-5291.

Respectfully submitted,
MORGAN & FINNEGAN, L.L.P.

Dated: October 1, 2008

By: 
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